REMARKS

This is intended as a full and complete response to the Final Office Action dated August 14, 2009, having a shortened statutory period for response set to expire on November 14, 2009. Applicants submit this response to place the application in condition for allowance or in better form for appeal. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-28 are pending in the application. Claims 1-28 remain pending following entry of this response. Claims 9-28 have been amended.

Rejections under 35 U.S.C. §102(e)

The Examiner rejected claims 1-11 and 13-28 under 35 U.S.C. 102(e) as being anticipated by *Van Hook et al.* (US 6,342,892) (hereinafter *Van Hook*).

Claim 1 recites the limitation of a hardware-based Physics Processing Unit (PPU), comprising a vector processor adapted to perform multiple, parallel floating point operations to generate physics data, and a data communication circuit adapted to communicate the physics data to a host. *Van Hook* falls to teach or suggest these claim limitations.

First, Applicants submit that *Van Hook* does not disclose a vector unit capable of generating physics data. *Van Hook* discloses a video game system having a main processor 100 and a coprocessor 200 that handles audio and video signals through a signal processor. The coprocessor in *Van Hook* includes various sub-processors, such as a signal processor 400 and a CPU interface 202. The Examiner analogizes the signal processor 400 of *Van Hook* with the vector processor, as claimed. See page 3 of the Office Action. The Examiner also analogizes the main processor to the host, as claimed. See page 3 of the Office Action. The signal processor 400 of *Van Hook* includes a vector unit 420 that is configured to execute audio and graphics tasks. See *Van Hook*, column 16, lines 7-11. The vector unit 420 receives commands from the main processor interface and executes those commands only to process graphics and audio data. See column 18, lines 1-7 of *Van Hook*. However, *Van Hook* does not teach or suggest that the vector unit 420 or the signal processor 400 is capable of generating physics data.

Furthermore, Applicants submit that the signal processor of *Van hook* is not capable of performing multiple, parallel floating point operations to generate the physics data. In fact, *Van Hook* expressly states that the signal processor 400 does not perform floating point operations. See column 18, lines 58-59 of *Van Hook*. In the Office Action, the Examiner argues that a vector unit capable of performing fixed and floating operations if disclosed at column 12, lines 17-25 and column 18, lines 52-57 of *Van Hook*. However, column 12, lines 17-25 of *Van Hook* describe the main processor 100, while column 18-lines 52-57 describe the signal processor 400. In other words, Examiner analogizes both the main processor 100 and the signal processor 400 of *Van Hook* with vector processor, as claimed. Respectfully, Applicants submit that both the main processor 100 and the signal processor 400 cannot be the vector processor. Furthermore, Applicants submit that the Examiner has already analogized the main processor 100 to the host, as claimed. Accordingly, Applicants submit that the main processor 100 cannot be both the host and the vector processor.

As the foregoing illustrates, *Van Hook* fails to teach or suggest each and every limitation of claims 1 and 9. In particular, *Van Hook* fails to teach or suggest generating physics data and *Van Hook* fails to teach or suggest performing multiple, parallel floating point operations. Therefore, claim 1 and claims 2-8, dependent thereon, are in condition for allowance.

Claim 9 recites also the limitations of a vector processor that is adapted to perform multiple, floating point operations. Therefore claim 9 is allowable for at least the same reasons as allowable claim 1. Since claims 10-11 and 13-28 depend on claim 9, these claims are also in condition for allowance.

Rejections under 35 U.S.C. §103(a)

The Examiner rejected claim 12 under 35 U.S.C. 103(a) as being unpatentable over *Van Hook*, as applied to claims 9-11 above, in view of *Intel* (*Intel PCI and PCI Express*; note that the subject matter relied upon in the reference is dated) (hereinafter *Intel*).

Claim 12 recites the limitations of at least one data communications protocol of USB, USB2, Firewire, PCI, PCI-X, PCI_Express, and Ethernet. The combination of *Van Hook* and *Intel* fails to teach or suggest these limitations.

Intel discloses a physical interface and is completely silent regarding the generation of physics data. The Examiner relies on *Intel* only to teach the PCI and PCI-Express interfaces. Thus, *Intel* fails to cure the deficiencies of *Van Hook* set forth above.

As the foregoing illustrates, the combination of *Van Hook* and *Intel* fails to teach or suggest each and every limitation of claim 12 (or any of the other pending claims). Therefore, all of the pending claims are in condition for allowance over the references cited by the Examiner.

CONCLUSION

Based on the above remarks, Applicants believe that he has overcome all of the objections and rejections set forth in the Final Office Action mailed August 14, 2009 and that the pending claims are in condition for allowance. If the Examiner has any questions, please contact the Applicants' undersigned representative at the number provided below.

Respectfully submitted,

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